Abstract of the Disclosure

An apparatus and method for connecting a processor to buses. The apparatus includes a multiplexer which, when addressing information indicating the address of a first memory connected to a synchronous data bus synchronized with a processor, from the processor is received, receives first data from the processor and transfers the received first data to the first memory through the synchronous data bus, or receives second data from the first memory through the synchronous data bus and transfers the received second data to the processor, and if address information indicating the address of a second memory connected to an asynchronous data bus not synchronized with the processor, from the processor is received, receives third data from the processor and transfers the third data to a buffer, or receives fourth data from the buffer and transfers the fourth data to the processor.